PILOT SCALE PRODUCTION AND RELIABILITY TESTING OF SOLAR CELL MODULES BASED ON A LOW COST COPPER ELECTROPLATING PROCESS

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ABSTRACT: As silicon solar cell technology featuring screen printed silver paste continues to mature, the cost of the front side conductor continues to grow as a percentage of the overall manufacturing cost. A cell concept based on electroplated nickel and copper contacts offers a significant cost savings, as well as a benefit to cell efficiency through reduced shading and lower contact and line resistance. This work details a new, simplified metallization process featuring pico-second laser ablation of the ARC combined with single-sided plating from a novel, high-speed copper formulation. More importantly, we present the details of a low cost scale-up of the metallization process on high volume mass production tools, plus fabrication of industrial modules and reliability testing according to IEC specifications. Electrical and adhesion data is presented on a statistically comprehensive sample set, proving the benefits of the new contact structure. These data offer the combined benefit of improved efficiency, a sizeable reduction in cell materials cost, and a clear pathway for the implementation of the process on a mass production scale.
Keywords: silicon, wet chemical metallization, electrodeposition, cost reduction

1 INTRODUCTION

Screen printed silver paste has been the dominant front side metallization technology on silicon solar cells for years. Metallization featuring screen printed silver is a simple, well known process that is easily scalable for high volume production. However, even with further improvements in paste technology over the past few years, it is increasingly becoming a limiting factor in the overall economics of the cell. Cell efficiencies are restricted by the contact resistance of silver paste to the underlying emitter, which is further strained by a movement to lower dopant concentrations at the silicon emitter surface. Additionally, the screen printing process is approaching a practical limit in printed line width, which results in unwanted shading and a ceiling for J_{sc}. Finally, the cost of silver is an increasingly significant portion of the overall cell materials cost, as will be discussed later in this paper.

An alternative approach to conductor formation is through the use of wet chemical metallization, more specifically nickel and copper plated contacts. This is not a new technology, as it has been used in production for more than 10 years [1]. Plated conductors offer a number of advantages, including low material cost, excellent contact resistance and potential for higher cell efficiency. However, there have been a number of challenges associated with plating that have prevented wide scale implementation of the process to this point. This paper details an improved wet chemical metallization process that overcomes previous deficiencies and offers a pathway to industry adoption.

2 DIRECT PLATING ON SILICON

It is widely accepted that the photovoltaic industry will gradually adopt electroplated metal contacts over the coming years [2]. However, various methods of forming a plated conductor exist and no specific sequence of metallization steps has gained widespread adoption to this point [3]. In this paper, the authors have laid out a detailed package of materials, equipment and process, nicknamed here "PoSi," or direct Plating on Silicon. Figure 1 demonstrates how the PoSi process can be integrated into a traditional crystalline silicon cell production scheme.

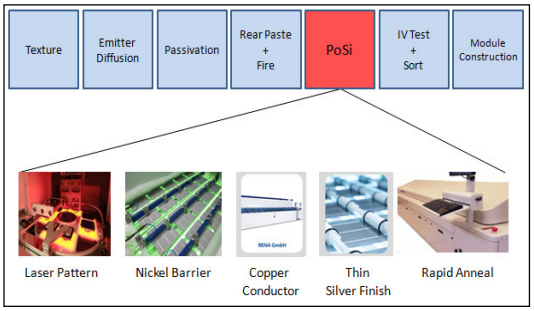

Figure 1: Schematic demonstrating the integration of the PoSi process into an existing p-type Al-BSF cell production line.

The core of the PoSi process is a replacement of standard front side screen printed metallization steps with a new process flow featuring wet chemical metallization. In this example, the equipment and process steps of front side printing, drying, and firing are replaced by a laser tool, wet chemical metallization module, and an annealing furnace, all inline. The substitution of the PoSi process steps for the traditional front side metallization sequence should not add considerably to the overall footprint of the cell fabrication process, but it will add value in the form of efficiency improvements and cost savings, as detailed below.

The first step in the PoSi process is patterning of the wafer surface by laser ablation. A high volume production tool has been developed which quickly and reliably ablates the silicon nitride anti-reflective coating on the wafer surface without damaging the underlying emitter. The use of a highly optimized pico-second pulse length is a marked advantage over the previous nano-second pulse length. Nano-second laser ablation had a

tendency to melt the silicon surface and cause damage to the emitter junction, whereas newer laser technologies can pattern the cell with minimal damage (figure 2). The laser tool is able to quickly ablate a contact pattern featuring fingers of 5-15 µm width.

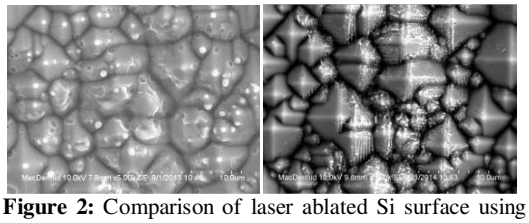

Figure 2: Comparison of laser ablated Si surface using nano-second (left) and pico-second (right) pulse lengths. Tops of pyramids are melted by nsec laser ablation, while the psec laser leaves a "nano-roughened" texture.

After laser patterning, the wafer proceeds to the wet chemical portion of the PoSi process. Following a short pretreatment step to remove any oxide on the ablated silicon surface, the cell is plated with nickel in a single-sided process by a light induced plating (LIP) mechanism. Nickel is plated first because it forms a low resistance contact to silicon, and because it is an excellent diffusion barrier to copper. This ensures that copper will be unable to diffuse into silicon and cause shunting of the diode junction.

The cells are then plated with copper in the same LIP manner, using a previously reported novel plating chemistry [4]. Copper is the primary conductor material, as it has comparable conductivity to silver at a much lower cost. A smooth copper deposit is able to be deposited at high speeds (figure 3), thus shortening the footprint of the plating tool. Additionally, the smooth and rounded nature of the copper deposit allows for greater internal reflectance of light, and subsequently lower effective finger width [5]. After copper, the cells proceed through a final plating module and a thin (0.2-0.3 µm) silver finish is applied by immersion deposition. The silver capping layer serves to prevent oxidation of copper, and preserve solderability during the module construction stage.

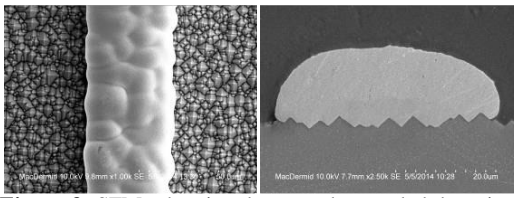

Figure 3: SEMs showing the smooth, rounded deposit of electroplated copper fingers on top-down (left) and cross-sectional (right) images.

The final step in the PoSi process is a rapid thermal annealing step. The cell is conveyed through a commercially available belt furnace under inert atmosphere and exposed to a moderate thermal annealing profile. This thermal step serves to form a nickel-silicide intermediate layer, which improves contact resistance of the plated conductor and also improves adhesion.

It is worth reiterating the advantages of the PoSi process over the incumbent technology. Laser ablated and plated contacts are only 30-40 µm in width fully plated, which is a significant improvement over screen printed paste (~60 µm), and allows for higher Jsc and cell efficiency. Plated conductors offer a full area contact with the doped silicon, in contrast to the intermittent contact of sintered paste/glass. Electrical conductivity of electroplated copper is better than fired silver paste composed of porous silver flake. Additionally, plated cells enable lower surface dopant concentrations, represented by sheet resistances in excess of 120Ω/sq. Emitters featuring low dopant concentrations reduce the inefficiencies of charge-carrier recombination at the cell surface. Finally, the importance of a single-sided plating process must be stressed. It is well known that plating electrolytes can corrode or damage rear side metal layers if they come into contact. This is especially true for Al-BSF, and the metal-oxide glass interface created by firing silver paste. By plating conductors on the front side of the wafer while not exposing rear side paste to the electrolytes in question, the greatest benefit from a wet chemical metallization process can be realized.

2.1 Cost considerations

One of the primary motivations for this project is the cost of silver paste. Plated cells replace screen-printed silver paste in the cell's build-of-materials (BOM) cost. State of the art cells consume 100 mg of front-side silver paste. The price of paste fluctuates with the price of silver, which traded in the range of $0.48-$1.57 per gram in the five years ending September 2014. At the time of this writing, 120 mg of paste cost ~$0.09 per cell. Copper metal, at $0.007/g, plus the very thin quantities of nickel and silver, sum to less than $0.035/cell. The material cost savings, plus benefits of increased power, can produce per cell benefits more than $0.10. The benefits for a 100MW production line overcome the expense of the necessary capital equipment costs in less than 18 months. Additionally, a transition to plated conductors removes the uncertainty caused by the volatility in the price of silver. By not depending on silver, cell manufacturers are not bound by the spot price in silver and associated supply/demand dynamics. This will become even more critical as expansion of photovoltaic production increases the worldwide demand for silver.

2.2 Challenges of plating

To this point, there have been noted challenges to adoption of plated conductors in mass production. Adhesion of plated contacts has typically suffered, especially after industrial soldering and module interconnection processes. Also, the long-term reliability of plated conductors has been questioned. This is primarily due to the fear of copper diffusion into silicon, which can be aided by the high temperatures a module can be exposed to daily. Finally, a comprehensive package of equipment and chemistry had yet to be developed and put together for this application. The authors believe they have identified a unique set of tools and chemical solutions to consistently plate metal contacts with excellent efficiency, mechanical properties and reliability.

3 EXPERIMENTAL

For the pilot scale production process detailed in this paper, approximately 600 commodity wafers were procured from a leading industrial cell supplier. The cells

were p-type CZ-Si wafers that were removed from the conventional production process after printing and firing of the rear side Al-BSF (see figure 1). The cells feature a standard 65 Ω/sq. emitter and high surface concentration of phosphorus. Front side passivation is achieved by deposition of a silicon nitride anti-reflective coating. The cell supplier also provided us with wafers from the same lot featuring front side screen printed and fired silver paste conductors to be used as a reference in module reliability testing.

3.1 Cell processing

The precursors were processed according to the PoSi schematic detailed in figure 1. A high speed laser tool was ablated the dielectric layer on the front surface of the cell in the pattern which is plated in subsequent steps. The use of a pico-second pulse frequency allowed a narrow finger opening of 15-20 µm without damage to the underlying emitter. After the cells were laser patterned, they were loaded into a high volume conveyorized wet chemical metallization line. The cells went through pretreatment, LIP nickel and copper, then received a thin immersion silver coating, as detailed earlier. After plating was complete, the cells proceeded through a short annealing step to improve contact resistance and adhesion.

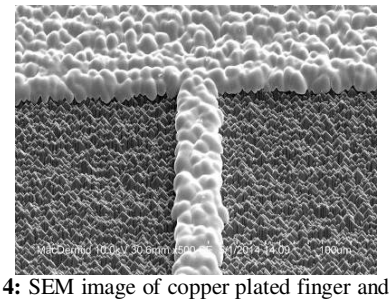

Figure 4: SEM image of copper plated finger and busbar fabricated during the trial.

3.2 Module fabrication and reliability

Following PoSi processing, IV characterization data was measured on the plated cells. The average results for approximately 400 plated cells appear in table I. The IV characteristics for this test group are exceptionally good, considering the cells came from a commodity production process, had a standard emitter diffusion profile, and rear Al-BSF. With an improved emitter diffusion profile and rear surface passivation (PERC), efficiencies nearing 21% have been achieved [6].

After IV characterization and sorting, the plated wafers were sent along with screen printed reference cells to Fraunhofer ISE for module fabrication and reliability testing. The cells were tabbed, strung and laminated into 60 wafer modules using standard ribbons, flux, and automated module construction tools. The modules were then characterized and subjected to reliability testing according to IEC specification 61215.

Table I: Average IV data from 400 cell PoSi plating experiments.

Voc (mV)	Jsc (mA/cm^2)	FF (%)	Efficiency (%)
640	38.1	80.3	19.6

4 RESULTS

4.1 Adhesion

After plating, annealing and characterization, a set of plated cells was removed from the processed group for adhesion testing. The wafers were spot soldered using a commercially available solder-coated copper ribbon (1.5 mm X 0.15 mm, Sn/Pb/Ag 61.8%/36.2%/2.0% coating) and low-acid solder flux. The cells were then peeled at a 90° angle using an automated strength gauge tester. Thirty-six maximum peel values were obtained for each cell. Figure 5a shows a representative "N vs. distance" graph collected during the peel of each busbar. Figure 5b features two box plots showing the distribution of peel strengths (in Newtons) and the mean peel result of both the current 2014 PoSi process, and a sample of last year's results for reference. The 2013 cell adhesion results suffered in comparison due to the use of a nano-second laser ablation process and non-optimized plating chemistry. The current process of record benefits from pico-second patterning, an improved chemical process flow, and an annealing step.

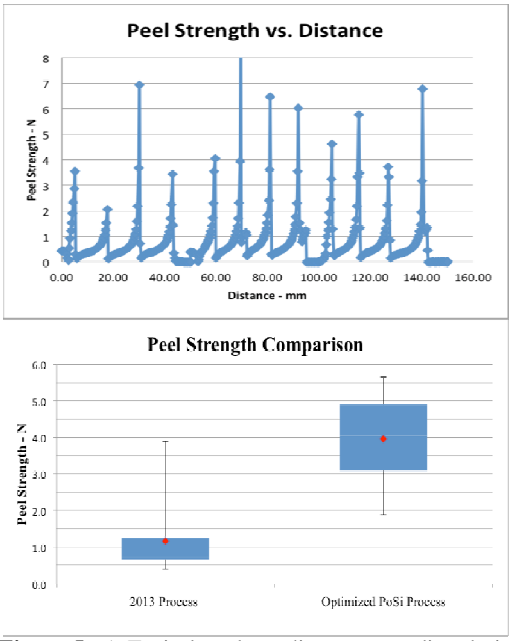

Figure 5: a) Typical peel vs. distance recording during the adhesion testing of cells plated in this trial, demonstrating maximum peel force in N. b) Box plot comparing the peel strengths data for 2013 process vs. the new, optimized PoSi process of record.

Figure 6 is an image of the ribbon and busbar after adhesion testing of this test group of cells. The failure mechanism is demonstrated to be cohesive within the silicon, indicating that the bond of the plated metal stack to the silicon substrate exceptionally high. Also, please note that we glued down the cells to an immovable laminate base for these peel tests. This is why no cell fracture and "silicon rip-out" is experienced, and why some of the peel results in the graph are greater than 5 N.

Figure 6: Example of a peeled busbar, demonstrating fracturing within the silicon substrate. Cells were glued down in order to observe this failure mechanism.

4.2 Reliability

Cells underwent an industrial tabbing and stringing process, were laminated into modules, and then were exposed to thermal cycling and damp-heat testing according to IEC 61215. Full modules constructed from screen printed silver paste on the same precursors served as controls in the IEC accelerated age tests. As shown in the results, both groups of modules were comfortably within the IEC 61215 degradation limit of -5% power loss. The data suggests that the cells maintained the integrity of the metallized stack through thermal cycling and damp-heat testing, and also there was no diffusion of copper into the silicon, which would have led to shunting and subsequent power loss.

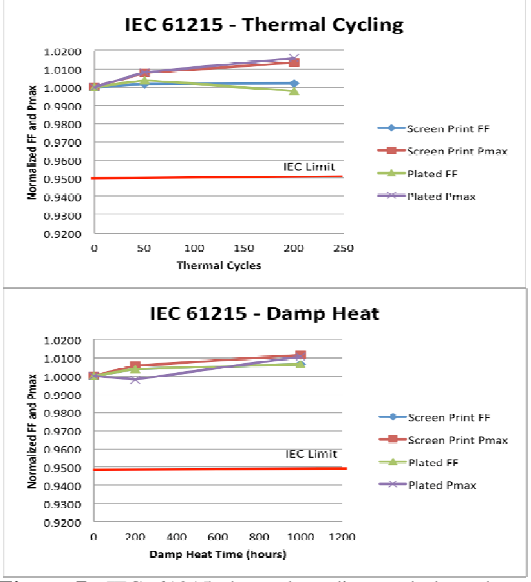

Figure 7: IEC 61215 thermal cycling and damp-heat reliability testing of modules featuring plated conductors, as measured at Fraunhofer ISE

5 CONCLUSIONS

In this work, a simple process has been presented and demonstrated to replace screen printed silver paste with laser patterned and electroplated metal contacts. The implementation of a pilot scale production sequence demonstrates the ability to scale the process into mass production. Adhesion and reliability data also confirm the process is ready for industry adoption. Metrics that prevented large-scale adoption of copper conductors on silicon in the past, such as adhesion, efficiency, cost, and equipment size, were overcome, as proven in this successful scale-up. The application of lowly-doped emitters, optimized finger spacing and rear side passivation techniques should prove to afford even greater efficiency benefits in combination with the PoSi process going forward.

Figure 8: module constructed and tested at Fraunhofer ISE

6 ACKNOWLEDGEMENT

The authors would to thank Motech Industries, Inc. for supporting this project by supplying precursor cells for plating as well as screen printed reference wafers.

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