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Copper plating process for filling micro vias and through via holes with minimum surface deposition

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About the author

Maria Nikolova is a Senior Research Fellow at MacDermid, Inc., Electronics Solutions in Waterbury, CT, U.S.A since 2003. She holds a Ph.D. in Chemistry, 1988.
She has developed new technologies for the electronic industry applications including via fill, PTH, and high throw copper electroplating. Maria Nikolova participated and supported installation of new technologies in North America, Asia, and Europe.
Before joining MacDermid she was a Senior Research Scientist at The John Hopkins University, Baltimore, MD, Materials Science and Engineering Department. She investigated the deposition of metals and alloys. She also studied fabrication of nickel nano-filaments cathode arrays by electrochemical methods for panel displays.

M. Nikolova is an author of more than 42 technical papers and holds 12 patents.

Copper Plating Process for Filling Micro vias and Through via Holes with Minimum Surface Deposition

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ABSRACT

This paper addresses the challenges of the miniaturization in the PCB manufacturing that enables more functionality in the same or less space. Copper is used in the manufacturing of many electronic devices due to its electrical and thermal conductivity properties and the possibility of electroplating. Copper plating solutions are used for fabrication of PCBs and semiconductors. In particular electrolytic copper has been widely used for filing micro vias, being an important technology in the fabrication of high density interconnections (HDI) of PCBs and IC package substrates. Efforts are being made to completely fill through via holes in build-up core layers in HDI and IC with void free solid copper. This has been associated with improved thermal and mechanical properties as well as with increased reliability and reduced cost.

The purpose of this study is to provide a new electroplating copper system that fills small features as well as forms a uniform surface copper plating coating which meet the recent requirement for low surface copper thickness up to 15 µm. In addition to that copper plated on the board surface is to be bright and leveled. Direct current, DC plating is performed in a copper bath containing high copper and low acid concentration. High CDs used allowed for a faster filling speed with high throughput. The functions of the organic additives are discussed. Factors affecting filling capabilities, dimple formation, and void formation are shown. Properties of copper film as well as the structure of plated metal are studied. The process can be used with soluble copper anodes or with insoluble anodes and it is applicable for VCP, Vertical Continuous Plater.

INTRODUCTION

The trend of portability combined with increased functionality of electronic devices has driven the miniaturization of PCBs. Electrolytic copper plating is used in a variety of industrial applications such as electronic industry, in particular for the fabrication of printed circuit boards, PCB and semiconductors [1-3]. Copper is electrodeposited over the selective portion of the surface of PCB into blind vias and onto the walls of through holes. For semiconductor application copper is deposited onto the surface of a wafer containing a variety of features such vias, trenches and combination of them. For High Density Interconnects new approaches have been developed such as sequential build up technologies, which utilize blind vias. An important objective in technologies that use blind vias is maximizing via filling while minimizing the thickness and thickness variation of copper deposit across the substrate surface. The need of improved thermal and mechanical properties in combination with improved reliability has lead to work on filling through via holes in build-up core layers in HDI and IC with solid electrodeposited copper. The PCBs production trends include deployment of more micro-vias to more constructions, smaller micro-vias in most uses, and copper filling of through holes for substrates / cores.

ACID COPPER PLATING PROCESS

A typical copper plating solution contains copper sulfate, sulfuric acid, chloride ions, and organic additives that control the deposition process and the quality of the plated coatings [4-6]. Various organic compounds are used in plating baths during the production of PCBs, chip carriers, and semiconductors [7, 8]. They act as levelers and brighteners enabling as uniform a deposition of copper as possible on different regions of the PCB including through holes and BMVs. The purpose of this work was to determine the effect of the organic additive species, their

concentration as well as the processing parameters on via filling. In general there are three basic additives that are used in acid copper electroplating baths: Wetter, Brightener, and Leveler. The Wetter (suppressors, high molecular weight polyether compounds and polyoxyalkylene glycols) in the presence of chloride ion has a strong polarizing influence producing a large decrease in the exchange current density. Addition of Brightener such as sulfopropyl sulfides to an acid copper electrolyte acts as a depolarizer producing an increase in exchange current density. As an example, the maximum depolarization effect for SPS (disodium bis (sulfopropyl) disulfide) was observed at a concentration of about 5 ppm. Above this concentration of the brightener, the surface blocking effect of the adsorbed brightener mitigates the depolarizing effect to some degree. The brightener spices are much smaller molecules than the wetter molecules and so the adsorption of the wetter does not appear to significantly interfere with the adsorption of the brightener. Leveler adsorbs preferentially near the most negatively charged sites of the cathode (PCB), thus slowing down the plating rate at high current density areas. The organic additives affect the secondary and tertiary current distribution and control the physical mechanical properties of the metal deposits.

BLIND MICRO VIA FILLING

The paper describes a new copper plating process that can deposit an even and smooth copper plating film, preferably with bright appearance with minimal surface copper thickness. Reduced cycle time by utilizing higher CDs increases productivity. The process is applicable for any layer via constructions. Physical mechanical properties of deposited copper meet IPC specification.

Via Fill Copper plating bath constituents are given in Table 1.

Component	Target	Range
Cu as metal	55 g/l	50 – 60 g/l
Acid	60 g/l	40 – 60 g/l
Chloride	55ppm	50 – 60ppm
AVF 100 Wetter	9 ml/l	8 - 12 ml/l
AVF 100 Brightener	2 ml/l	1.5 – 3 ml/l
AVF 100 Leveler	4 ml/l	3 – 8 ml/l
Temperature	22°C	20 - 24°C
Current Density	0.8 – 2.0 ASD	0.5 – 2.5 ASD

Table 1 - Bath constituents

The steps included in process sequence are shown in Table 2:

Acid Cleaner, 3 min
Rinse, 2 min
Micro etch, 40 sec
Rinse, 2 min
Acid dip, 1 min
Via Fill Bath

Table 2 – Process flow

Fill ratio

The Fill Ratio is defined as the ratio B/A in percents as shown in Figure 1.

Fill Ratio = B/A x100. The acceptable value of the Fill Ratio is 80% or higher.

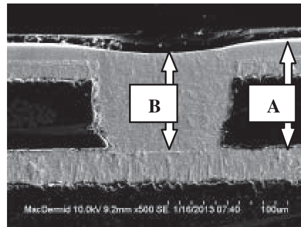

Figure 1 – Fill Ratio

Blind Micro-via Filling Results

Filling Process

Figure 2 and Figure 3 show filling process for two technologies. The newly developed technology, Advanced Via Fill – AVF 100, allows for a shorter plating cycle to be used and for faster filling of the vias than the existing VF 300 one. The thickness of copper deposited on the surface is lower when AVF 100 is used.

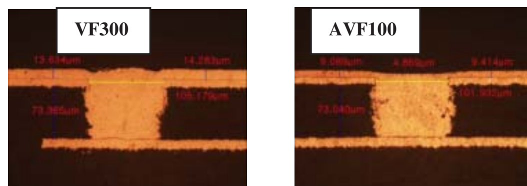

Figure 2 – 100 µm diameter x 75 µm depth vias

VF 300	**AVF 100**
Plating time: 50min	**Plating time: 40min**
Surface Thickness: 14µm	**Surface Thickness: 9µm**

Figure 3 demonstrates via filling process as the time progresses for the two processes studied. AVF 100 process has advantages as compared to VF300 process being faster and giving a thinner surface copper thickness.

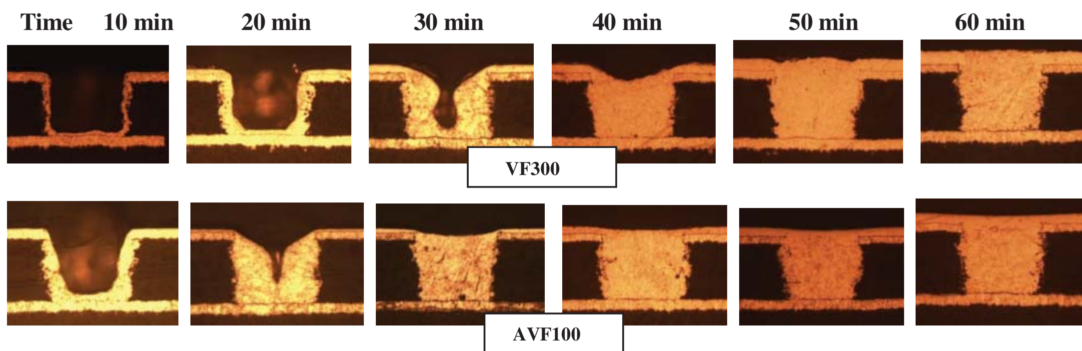

Figure 3 – Filling of 100 µm diameter x 75 µm depth vias as a function of plating time

The process described was used to plate various diameters vias 75 µm and 100 µm deep. Examples are given on Figure 4. All vias sizes were plated simultaneously. Vias were filled with = > 80 Fill Ratio, voids free. The dimple depth were = < 10 µm. The surface copper was in the range 10 – 15 µm.

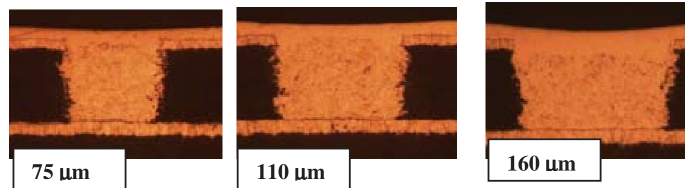

Figure 4 – Filling various diameters vias 75, 110, and 160 µm; depth 75 µm

Effect of Plating Component on Via Filling Performance
Inorganic Component Concentration
The effect of copper sulfate is shown of Figure 5. It was found that higher concentration of CuSO4x5H2O has positive effect on the filling of larger diameter vias. Smaller diameters vias are filled up at higher as well s at low copper sulfate concentration. H_2SO_4 and HCl concentration does not have significant affect on filling process.

Concentration	110µm	120mm	140mm	Notes
CuSO4 / H2SO4 / HCl 260g/L / 40g/L / 50ppm Br/Le/We : 2/4/10 1.2ASD 60min				All size via-hole Flat (No Dimple)
CuSO4 / H2SO4 / HCl 240g/L / 40g/L / 50ppm Br/Le/We : 2/4/10 1.2ASD 60min				Under 120µm Via-hole Flat (No Dimple)
CuSO4 / H2SO4 / HCl 220g/L / 40g/L / 50ppm Br/Le/We : 2/4/10 1.2ASD 60min				Under 110µm Via-hole Flat (No Dimple)
CuSO4 / H2SO4 / HCl 200g/L / 40g/L / 50ppm Br/Le/We : 2/4/10 1.2ASD 60min				Under 110µm Via-hole Flat (No Dimple)

Figure 5 – Effect of copper sulfate concentration on via filling

Organic Additives Concentration

The bath filling performance depends on organic additives nature and their concentrations. Leveler has a significant effect on via filling. Brightener does not affect the filling if higher than 1 ml/l. Wetter does not have an effect on via filling within a wide concentration range. The optimum concentrations for filling vias was found to be: Brightener 1.8 - 2 ml/l, Leveler 4-5 ml/l, and Wetter 9 -12 ml/l.

Agitation

High flow contributes to dimple formation. The dimple is deeper at higher flow rates. The results from the study are shown on Figure 6.

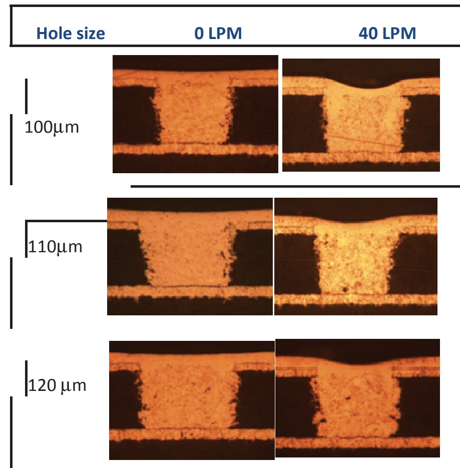

Figure 6 – Effect of agitation

The flow rate that is used during the deposition process can be adjusted depending on via size and filling requirements.

Thermal Reliability

Solder shock resistance testing per IPC TM-650 2.6.8 was used to study the thermal characteristics of plated boards. Solder shock conditions were 10 second float at 288ºC for 6 times. The thermal integrity was excellent for all of the via sizes plated. No cracks were observed as shown in Figure 7.

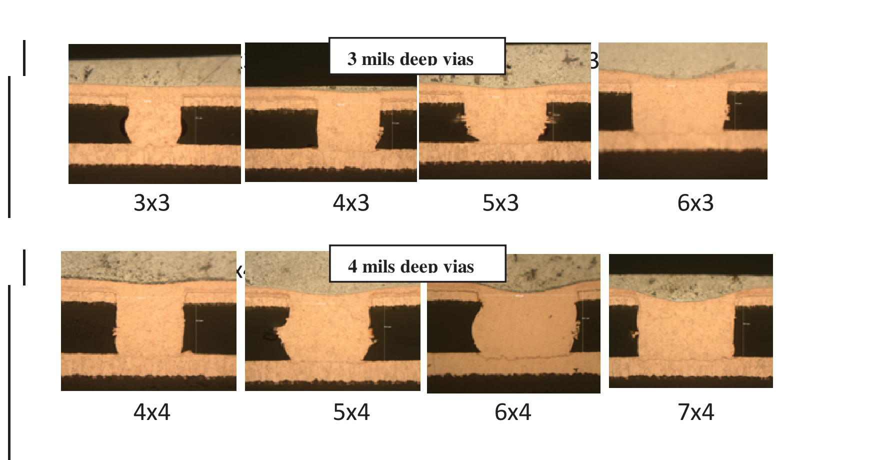

Figure 7 – 6x Solder Shock

Structure
Deposits plated from this electrolyte were bright and leveled. SEM pictures were taken from copper surface to examine the surface morphology. Figure 8 shows copper deposited on the surface of the panel from a perpendicular view. It reveals small equiaxial grain size structure. No particular texture was determined.

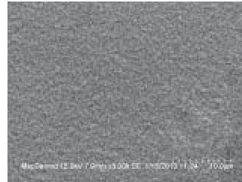

Figure 8 – Surface morphology, SEM 5000x

Cross section pictures are shown on Figure 9. An etch solution was used to expose the crystal structure of the deposit. Small grain structure is observed.

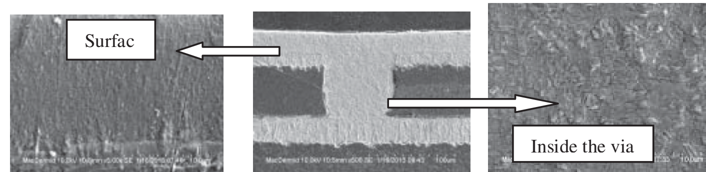

Figure 9 – SEM Cross Sections pictures

Summary for Blind Micro-Via Filling
The described technology for advanced via filling is designed for very low surface copper. The main characteristics of this technology are:

- Excellent blind microvia fill performance with thin copper deposition thickness =< 15 microns for enhanced fine line resolution
- Designed for any layer via constructions
- Faster filling speed for more efficient equipment utilization and reduced cycle time
- Reliable thermal performance
- Highly leveled, bright surface
- All bath additive components can be monitored by CVS

FILLING PILLARS OR BUMPS ON SUBSTRATES
Electroplate Pillar Plating Process
The Electroplate BMP Pillar Plating Process has been studied. This DC acid copper plating system is designed for photo defined pillars plated onto plastic chip carriers. It is a high speed plating process 4.0-9.0ASD giving uniform pillar height and it is applicable for Vertical Continuous Plater.

The process combines the use of a copper activator with an electrolytic copper bath. The copper activation step is a combination of sulfuric acid and an additive used to ensure uniform pillar height.

Dry-Film Process
This is a crucial and important step in the process.
The bumps are photo defined with a plating resist. This resist is typically thicker than standard plating resist used in the conventional PCB manufacturing and can be applied in a single or multiple pass through dry film lamination

process. Dry film residues that are not removed from the base copper surface will result in low bump thickness or no bump plating at all.

Wetting of the Photo Defined Bump Areas

The aspect ratio of the intended plating areas may be up to and beyond a 1:1 aspect ratio. Plating resist by its very nature is hydrophobic (non-polar) and repels aqueous solutions, making “wetting” of the photo defined area more difficult. Proper cleaning chemistry, with low surface tension, is needed to ensure complete wetting of all holes.

Base Copper Activation

The base copper which will be plated must be dry film residue and oxide free. Uniformity of pillar height relies on quick and simultaneous copper plating initiation of all photo defined areas. The optimized process ensures immediate plating initiation, yielding uniform bump/pillar height across the substrate.

Plating Results

Figure 10 demonstrates plating of 100 and 130 microns diameter pillars.

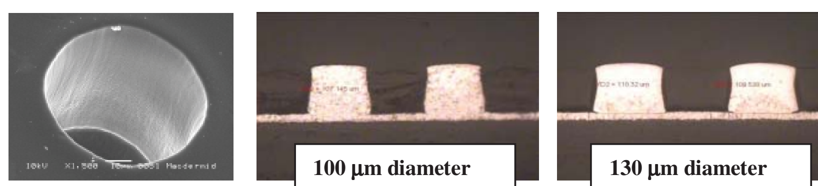

Figure 9 – Plating of 100 microns deep pillars

THROUGH HOLE FILLING FOR HDI AND IC SUBSTRATES

The results from the study were used further in developing a new process for filling through micro vias. Filling through via holes by copper electroplating started to develop recently to benefit the fabrication of printed circuit boards (PCBs) with high-density interconnections (HDI) [9] and three dimensional (3D) chip stacking [10]. Copper electro-deposition to fill through vias is particularly beneficial for the latest package substrates designs. Through vias filled with copper has the advantage over any type of resin material available, due to copper thermal and electrical characteristics being significantly better. The CTE of the copper-filled core is dependant only on the copper metal and the glass-reinforced resin of the drilled dielectric. The benefits of using copper through via filling process include increased productivity and reduced overall cost.

There are differences between the plating processes for filling blind micro-vias and through vias due to the differences in the geometric shapes. The differences include the hydrodynamic conditions, solution flow in and out of the through vias. Copper could be deposited in a center-up mechanism, as opposite to the bottom up mechanism in case of blind micro vias. The final plating results depended on the bath chemistry as well as on the plating parameters.

Plating Results

The cross section coupons were taken from the plated boards. Figure 11 shows the result of a DC plating in the same solution, first to bridge and then to fill up the holes. The deposition rate on the hole walls, hole corners and on the surface depends on the plating conditions and hole geometry. As opposite to the BMV filling up, this rate was found to be higher in the center of the hole at the earlier stages of the plating. As the plating process continued further, the top and the bottom parts of the hole were filled up void free.

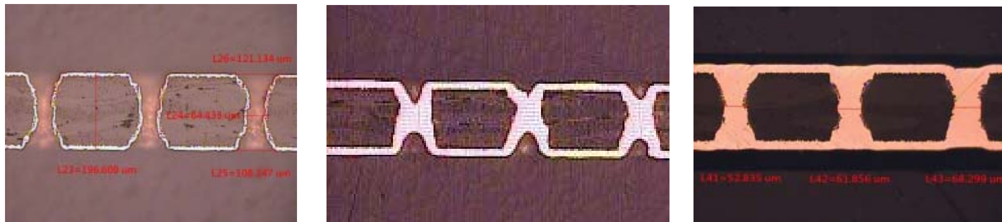

Figure 11 – Through Hole Fill in Panel Plate

Pattern plate is shown on Figure 12. Plating was performed in a solution containing copper sulfate 220 - 250 g/l sulfuric acid 55 g/l, chloride 60 - 80 ppm, Brightener 1.2 – 2.5 ml/l, Wetter 8 - 20 ml/l, Leveler 1.5 – 2.ml/l

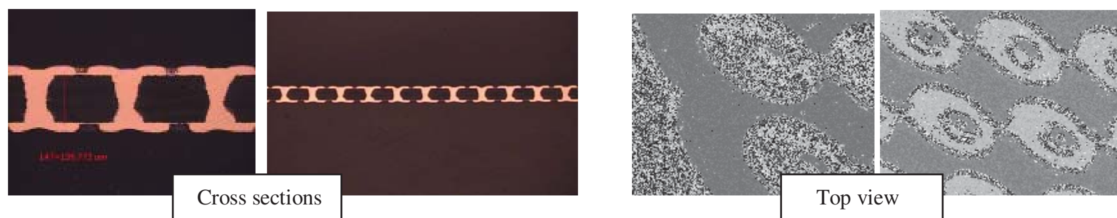

Figure 12 – Through Hole Fill in Pattern Plate

The efforts were directed toward reducing the surface copper thickness. A thin surface copper plating was achieved in a case study with X shaped through holes. The center up filling mechanism was enhanced by the hole geometry resulting in a faster hole filling with less copper deposited on the board surface, as shown in Figure 13.

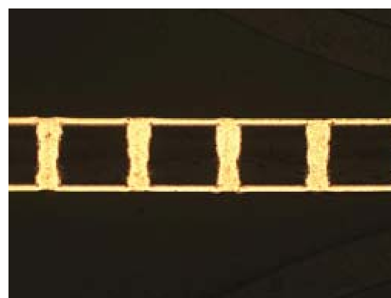

Figure 13 - 60 µm diameter filled up through vias in 200 mm thick substrate, DC plating

Two steps DC plating process was used for more difficult geometries. Figure 14 shows through hole fill with mechanical drill. Substrate thickness: 0.15 mm, through hole diameters: 75, 100, and 150 µm.

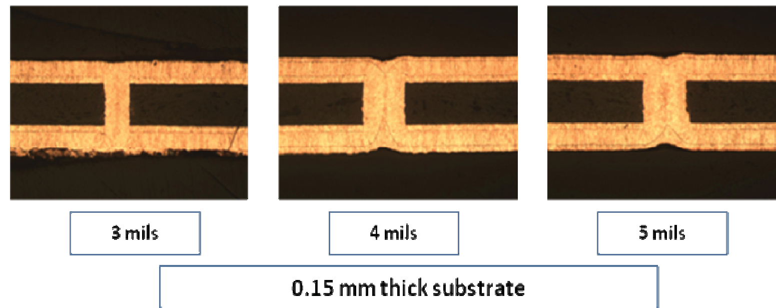

Figure 14 – Through Hole Fill by a two step process

This innovative technology is at an early stage. It is at the process of further adjustments, chemistry and current regimes optimization to enable a variety of HDI and IC substrate package designs.

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