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ELECTROPLATING PROCESSES FOR IC SUBSTRATES – EMBEDDED TRACE PLATE, VIA FILL AND THROUGH HOLE FILL

Saminda Dharmarathna [a], Maddux Sy [b], Benjamin Chao [b], Ivan Li [b], William Bowerman [a], Jim Watkowski [a], Kesheng Feng [a]

[a]MacDermid Enthone, 227 Freight Street, Waterbury, CT 06702

[b]MacDermidEnthone Global Development Application Center Taiwan
No. 16-1 Songjiang N Rd, Zhongli District, Taoyuan City, Taiwan, R. O. C. 320

kesheng.feng@macdermidenthone.com

ABSTRACT

The exponential advancement in the electronics industry has brought the PCB (Printed Circuit Board) world and IC/semiconductor world closer and closer. The platform serves as the connection between IC- chip and the PCB is called the IC substrate. In which, the connections are through a network of conductive Cu traces and through holes. Which represents the highest level of miniaturization in the PCB technology. In the era of miniaturization, high yield, and low cost, IC substrates play a crucial role, by providing the desired connection density. In order to utilize the maximum substrate real-estate, the distance between Cu traces also known as line and space (L/S) should be minimum. Typical PCB technology consist of L/S > 20 µm, whereas more advanced wafer level technology comprises of ≤ 2 µm L/S. In the past decade, the chip size has decreased significantly along with the L/S on the substrate. The scale mismatch and the smaller L/S distances creates unique challenges for both PCB industry and the semiconductor industry. Thus, Fan-out panel-level packaging (FOPLP), a new controversial technology has emerged. Still a very young technology, however current high volume production will justify further development of this emerging technology. Nevertheless, gaining momentum for these kinds of new technologies has driven the researchers to develop innovative solutions. Since the fine traces play an essential role in these emerging technologies, all the aspects of the fine lines are carefully considered when new plating solutions are developed. Plating uniformity, trace/via top planarity, which measures how flat the top of the traces and vias are few major features. These factors are extremely important when it comes to the multilayer processing, since the features of the prior layer could be transferred in to the successive layers. A non-planer surface could also result in signal transmission loss, distortion of the connecting points, like via and traces. Eventually cause short circuit and catastrophic failures. Therefore, plating solutions providing uniform, planer profile without any special post treatment are highly favorable.

Here we discuss innovative additive packages for DC Cu electroplating specially for IC substrates with capabilities in embedded trench plating, via filling and through hole filling with enhanced pattern plate capability. Figure 1. shows a typical pattern plate capability with dome shaped profile Vs the new innovative solutions with improved flat pattern profile.

The new solutions not only offer better trace profile, it also delivers via filling and laser-drilled through hole filling when the plating bath is controlled within the given parameters. Process optimization, thermal and physical characterization were also completed.

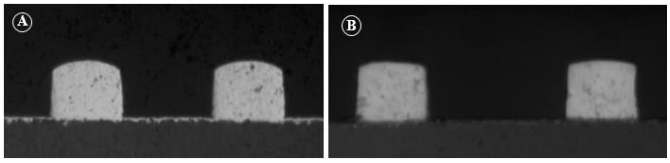


Figure 1. A: Typical pattern profile, B: improved pattern profile.

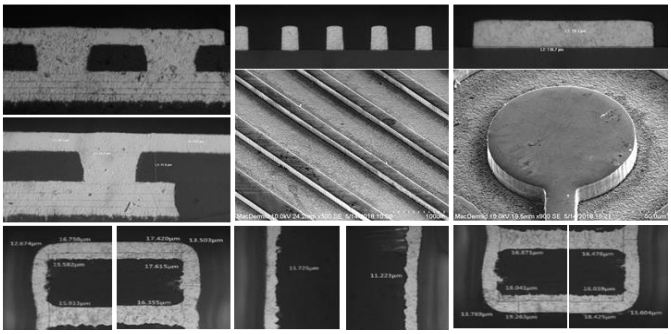


Figure 2. Capability of the innovative solution for simultaneous via fill and through hole plating with enhanced pattern plating.

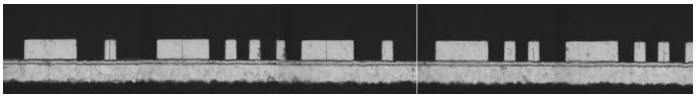


Figure 3. Capability of the embedded trench plating with uniform height between of pads and lines

KEYWORDS: Redistribution Layer (RDL), Embedded Trench, Via Fill, Pattern Plating, metallization, Planer Surface.

INTRODUCTION

High Density Interconnects and IC substrate package fabrication are two crucial areas driving miniaturization, speed, and portability of consumer electronics. Circuit density has grown immensely over the past few decades to meet today's printed circuit designs. Those designs include thin core material, fine line widths and smaller diameter through and blind vias. [1] As the technology evolves, there are more opportunities and means to add more components to the circuit board thereby achieving above mentioned qualities for electronics.

Fan-out panel-level packaging (FOPLP), a new controversial technology, relatively young, still need much understanding. Eventual goal being mounting chips directly on to PCB, however a RDL (redistribution layer) is still necessary to counter the scale

mismatch between wafer level and PCB level so far. Nevertheless, the cost and yield advantage of FOPLP technology will push the technology further. There are unique challenges for this new technology when it comes to formulate solutions to plate. The ever-decreasing L/S and unusual via aspect ratio make formulating more challenging. Here we introduce two processes to plate 2 in1 type of RDL to fill different sizes of vias with flat via top after filling and to plate trenches with flat profile and have very little deviation between pad and fine line areas.

ACID COPPER VIA FILL

Electrodepositions is the one of the crucial steps in developing a circuit board, this is where all the current routing network is plated on to the PCB board through traces, vias and through holes.[2] Copper is the choice of conductive metal due to several advantages such as cost and relatively high electrical and thermal conductivity. Therefore, usage of copper as an electroplating metal has grown massively over the last few decades. Advanced, proprietary board designs require cutting edge plating tools and innovative solutions to electroplate. These additives must be designed carefully to tailor the customer needs such as size of the vias to be filled, yield, surface Cu thickness, Cu distribution tolerance throughout the panel and the shape of the via after plating. Organic additives also control the plating rate and the physical properties of the deposit. With the correct additives and the plating tools customers now can achieve the desired plating needs. Plating tool plays a crucial role, with the unusual via geometries, conventional air agitation was not doing a justice to the additives. Therefore, within last few decades' impingement plating tools became a widespread tool among plating industry. Here we present two solutions to fill vias and plate trenches.

Copper via filling baths typically have high concentrations of Copper (up to 250 g/L Copper sulfate) and lower concentrations of acid (approximately 50 g/L sulfuric acid) to promote rapid filling. Typical systems will contain carriers (or wetters), brighteners, and levelers. In theory, it is possible to fill vias only with carrier and brightener. However, there are practical issues with two component systems like larger dimple size or even conformal fill.

Both carrier and leveler act as suppressors but in different ways and can be classified as different types of suppressors. Type I suppressors like carriers can be deactivated by the brightener whereas type II suppressors like levelers do not undergo deactivation. Carriers are typically high molecular weight polyoxyalkyl compounds [3]. They typically get adsorbed on the surface of the cathode and form a thin layer by interacting with chloride ions. Consequently, carrier reduces the plating rate by increasing the effective thickness of the diffusion layer [4]. Consequently, the energy level over the cathode surface topography is being equalized (same number of electrons locally for plating at any cathode surface spot) so that the resultant deposit becomes more uniform and evenly distributed.

Levelers typically consist of nitrogen bearing linear/branched polymers, heterocyclic or non-heterocyclic aromatic compounds being quaternized (positively charged). These compounds will adsorb selectively on high current density sites such as edges and corners, local protrusions and prevent copper over plating in high current density areas. [5]

On the other hand, brighteners increase the plating rate by reducing the suppression. They are typically small molecular weight sulfur containing compounds, also called grain refiners.

Tests were completed in 8-liter cell, as shown in Figure 4, and 200-liter pilot tanks. Insoluble anodes were used for higher applicable current densities, easy maintenance and a uniform copper surface distribution. Each bath was made up, dummy plated for 1 Ah/L, analyzed, adjusted to correct additive levels, and then the test panel was plated. Each test panel went through a pre-clean cycle of 1 min acid cleaner, 1 min rinse, 1 min 10% sulfuric acid before the plating.

Figure 4. Test cell 8 L with educator flow and knife agitation.

VIA FILL BATH CONDITIONS AND BATH COMPONENTS

Table 1 shows the operational conditions and optimum additive concentrations from a via fill chemical, SYSTEK UVF process, for larger vias, diameter up to 100 µm, and fine lines, down to 15 µm. Typical via fill baths have high copper and low acid to achieve the desired bottom up fill.

Table 1. Bath components and plating conditions.

SYSTEK UVF 100	Range	Optimum
Wetter	9 - 11 mL/L	10 mL/L
Brightener	0.5 - 1.5 mL/L	1 mL/L
Leveler	15– 25 mL/L	20 mL/L
Copper Sulfate ($CuSO_4$.**5** H_2O)	190 -220 g/L	200 g/L
Sulfuric Acid	40 - 60 g/L	50 g/L
Chloride Ion (Cl^-)	40 – 60 ppm	50 ppm

VIA FILL MECHANISM

The growth rate inside and outside a via is controlled by the additives. Additive compositions must be controlled in a set range shown in table 1 in order to get the desired "bottom-up filling". Analytical tools such as Cyclic Voltammetry Striping (CVS) analysis, and Hull cell plating are common utilized in the industry. Wetter molecules mainly adsorb on the surface suppressing the surface, while the leveler molecules adsorb selectively on to the negatively charged areas, due to the positively charged N group. This prevents over plating at the edges and avoids premature closure of the via leaving voids in the center of the via. Brightener being a small sulfur containing molecule diffuses faster into the via and accelerates the plating. During the plating process, the geometry of the via changes continuously, the brightener becomes concentrated inside the via causing a rapid plating in the via. This is called the curvature-enhanced-accelerator coverage (CEAC) mechanism. [6] Finally, when the via gets leveled with the surface and the plating

rates inside the via and on the surface become equal, the bottom up filling stops. However, depending on how strong the additive adsorbs and desorbs, the brightener may not diffuse as expected and the high concentration of the brightener will keep accelerating the plating and the momentum will over plate the via resulting in a "momentum pump" which is not desirable for IC substrate applications. Careful attention must be paid to the leveler and wetter suppression in order to obtain the desired flat top for both via and fine lines.

PROFILE% AND R VALUE CALCULATION

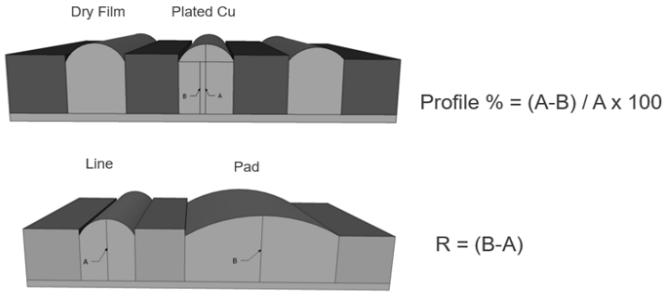


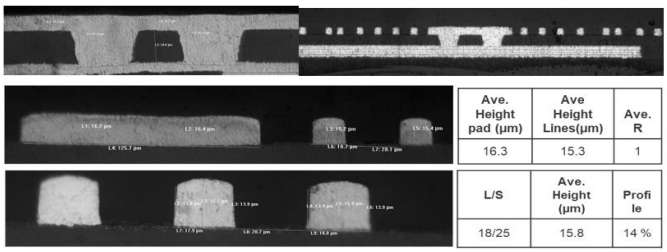
Figure 5. Profile % and R value calculation

Profile % is the amount of doming in the fine lines, the R value represents the height difference between pad areas and fine line areas which is a very important parameter for the embedded trench plating and the calculations are shown in Figure 5.

VIA FILL BATH PLATING RESULTS

Figure 6 shows typical plating performance from the via fill plating bath, SYSTEK UVF, planer via tops were obtained after plating. No additional chemical reduction is necessary. Lines and pads plated with this process showed only 14% profile for fine lines with line and space 18/25µm.

Doming was minimum for both line and pad areas. Also, the R value that is the difference between pad and lines was 1 µm. This process was specially designed to plate fine lines with high uniformity across the features and to fill large vias.



Ave. Height pad (µm)	Ave Height Lines(µm)	Ave. R
16.3	15.3	1

L/S	Ave. Height (µm)	Profile
18/25	15.8	14 %

Figure 6. Typical performance from SYSTEK UVF 100 plating

The via size in this application was 60 x 30 µm, which was easily filled from the plating process. With larger vias, up to 120 µm, it can be also filled well after the plated copper on the surface about 18 µm.

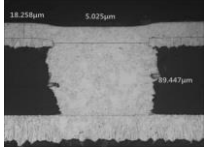
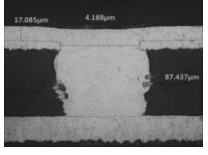
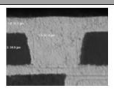
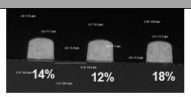
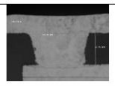
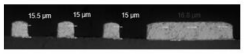
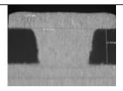
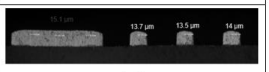
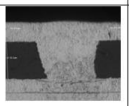
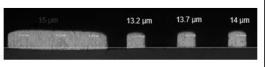
Via size	120 x 80 µm	100 x 80 µm
Plated thickness at 18 µm, dimple was below 5 µm		

Figure 7. SYSTEK UVF 100 plating for large size of vias.

A bath was aged up to 150 A/L and test platings were done at 50 Ah/L intervals. Results are tabulated in table 2. According to the results, stable performance was seen with flat via tops. Trace plating showed R value between 10-20% and the uniformity between pad and fine lies were between 1.5 – 2.0 µm.

Table 2. Bath aging test results, profile % for 18/25, L/S and R value, bath aged up to 150 Ah/L.

Age (Ah/L)	Via fill	Trace %	R
0			 1.6
50			 1.6
100			 1.4
150			 1.4

Physical properties of the plated deposit are essential for the reliability of the PCB. Tensile strength, elongation %, and internal stress are few most important properties. These properties show the tolerance of the deposit for thermal stress and warpage. The Cu deposit plated with additives, suppressor, grain refiner and leveler, will show characteristic physical properties. Standard equipment was used to measure the Tensile strength, elongation % and internal stress.

Figure 8 summarizes the results for Tensile strength, elongation % at two different bath ages, 1 Ah/L and 100 Ah/L. Tensile strength was above 45000psi and elongation % was above 23%, most importantly the properties did not change much during the bath ageing. Further proving the stable performance of the bath.

Internal stress in an important parameter when plating thin RDL, when there is too much stress the deposit may warp and warpage may be worse with time or with temperature. Figure 9 shows the internal stress data measured with the stress analyzing strips, both as plated strips and annealed strips at 130 °C for 1 h. The plated deposits exhibit low stress and the values did not change drastically as the bath age.

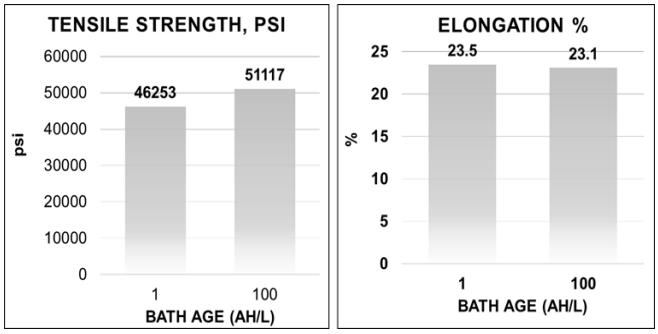


Figure 8. Physical properties, Tensile strength and elongation, fresh and aged baths

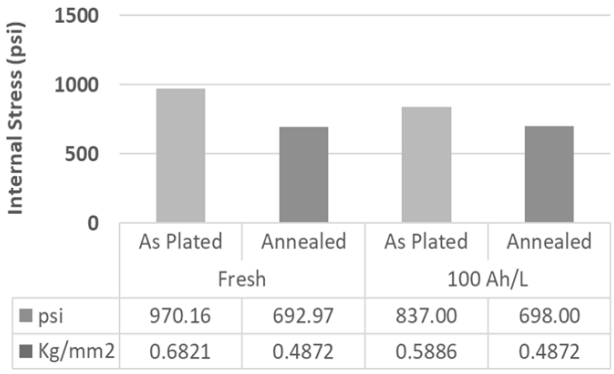


Figure 9. Internal stress of the Cu deposit plated, both as plated and annealed data for fresh and aged baths are shown.

EMBEDDED TRENCH PLATING RESULTS

As shown in figure 10, high degree of uniformity between pad areas and fine line areas was obtained from the plating bath for embedded trench, SYSTEK ETS process, under two different current densities 1.5 and 4 ASD. As expected low current density plating at 1.5 ASD gave better uniformity, 0.12 µm, and it was 0.74 µm under 4 ASD. The fine line features were down to 10 µm in the tests.

Table 3. Bath components and plating conditions.

SYSTEK ETS	Range	Optimum
Wetter	3 - 8 mL/L	5 mL/L
Brightener	2 - 3 mL/L	2.5 mL/L
Leveler	7 – 13 mL/L	10 mL/L
Copper Sulfate (CuSO4.5 H2O)	80 - 120 g/L	100 g/L
Sulfuric Acid	190 - 210 g/L	200 g/L
Chloride Ion (Cl-)	50 – 70 ppm	60 ppm

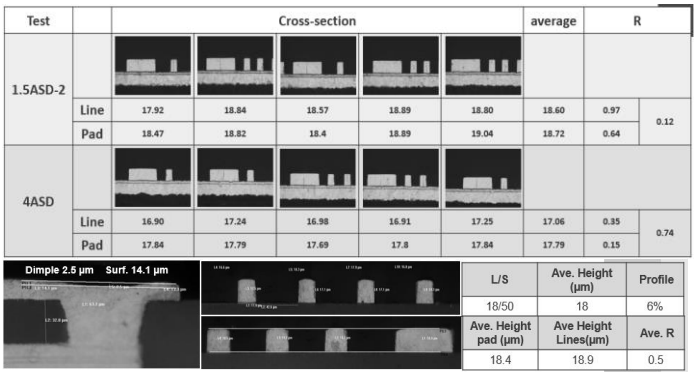


Figure 10. Typical Plating performance from ETS process

The SYSTEK ETS plating bath also has capability to fill via size at 60 x 30 µm with slightly dimple after the bath VMS was adjusted to 250 g/L CuSO4, 50 g/L acid, and 50 ppm Cl. This change in VMS did not have much effect on the profile %, profile shape or the R value.

The plated copper has great physical properties shown in figure 11. During the bath ageing the properties did not change significantly.

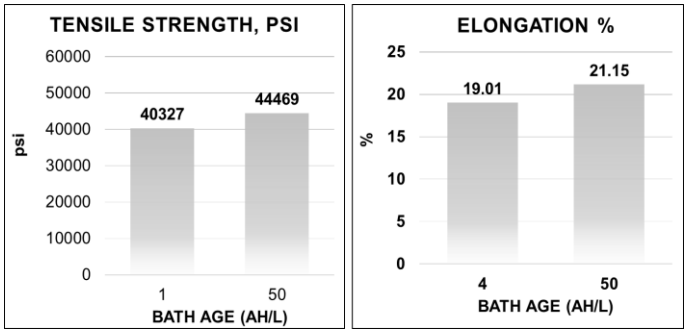


Figure 11. Physical properties, Tensile strength and elongation of fresh and aged baths from SYSTEK ETS process

CONCLUSION

Here we present the processes on acid copper via fill applications for IC substrates. The objective was to get planer via fill and flat profile for fine lines, and higher uniformity for embedded trenches between the pad height and fine line height. Formulations reported here showed excellent via fill capability and fine line profile% from via fill plating chemical. Outstanding uniformity was obtained, between the height differences of pad areas and fine line area, from the ETS plating chemical. The physical properties, tensile strength and elongation passed IPC class III and stayed stable as the bath aged. Low internal stress was shown for both as plated and annealed samples. All the additive components can be analyzed with Cyclic Voltammetry Stripping instrument.

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